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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/668,562
Filing Date: September 23, 2003
Appellant(s): TIERNO, JOSE A.

David E. Shifren
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed on 06/05/2009 appealing from the Office action mailed on 10/31/2008.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| 5,222,101 | Ariyavisitakul et al. | 06-1993 |
| 5,260,836 | Yada et al. | 11-1993 |
| 2004/0062329 | Hsu et al. | 04-2004 |

| | | |
|---|---|---|
| 2003/0086339 | Dally et al. | 05-2003 |
| 2004/0243258 | Shattil | 12-2004 |
| 6,570,944 | Best et al. | 05-2003 |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 9-11, 13, and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ariyavisitakul et al. (hereafter, referred as Ariyavisitakul) (US 5,222,101), in view of Yada et al. (hereafter, referred as Yada) (US 5,260,836).

As to claim 1, Ariyavisitakul discloses a method of equalizing (see Fig. 1 and column 1, last paragraph) an input signal 101 received from a communication channel, comprising the steps of: generating at least one sampling from the received input signal based on a clock signal (see block 104 and column 10 last paragraph) (i.e. inherently by using a clock signal); and compensating for distortion associated with the communications channel based on at least a portion of the at least one generated sampling (see the abstract, lines 3-5). Ariyavisitakul discloses all the subject matters claimed in claim 1, except that the sampling clock is not related to the clock signal used

to recover data associated with the received input signal. Yada, in the same field of endeavor, shows a system (see Figs. 1A and 1B) comprising a sampling device 4, an equalizer 5, a data detector 6, and a PLL circuit 7. Yada discloses that a sampling clock of frequency $F_s$, is supplied to ADC 4 to sample the input signal. Yada further discloses that the data detector 6 (interpreted as the recovery circuit) is supplied with a clock signal generated by a PLL circuit 7 (see column 8, last paragraph). Therefore Yada teaches that the sampling clock is not related to the clock signal used to recover data associated with the received input signal. It would have been obvious to one of ordinary skill in the art at the time of invention to use a clock for sampling the received signal unrelated to the clock used for data recovery purposes to make the process of data recovery faster (i.e. without spending time on recovering the clock of the transmitter and by using receiver's local clock).

As to claim 11, Ariyavisitakul discloses an apparatus (see Fig. 1) for equalizing an input signal 101 received from a communication channel (see column 10, last paragraph), comprising: a memory 105; and at least one processor coupled to the memory and operative to: (i) generate at least one sampling from the received input signal (see block 104 and column 10 last paragraph) (i.e. inherently by using a clock signal); and (ii) compensate for distortion associated with the communications channel based on at least a portion of the at least one generated sampling (see the abstract, lines 3-5). Ariyavisitakul discloses all the subject matters claimed in claim 11, except that the sampling clock is not related to the clock signal used to recover data associated with the received input signal. Yada, in the same field of endeavor, shows a system

(see Figs. 1A and 1B) comprising a sampling device 4, an equalizer 5, a data detector 6, and a PLL circuit 7. Yada discloses that a sampling clock of frequency $F_s$, is supplied to ADC 4 to sample the input signal. Yada further discloses that the data detector 6 (interpreted as the recovery circuit) is supplied with a clock signal generated by a PLL circuit 7 (see column 8, last paragraph). Therefore Yada teaches that the sampling clock is not related to the clock signal used to recover data associated with the received input signal. It would have been obvious to one of ordinary skill in the art at the time of invention to use a clock for sampling the received signal unrelated to the clock used for data recovery purposes to make the process of data recovery faster (i.e. without spending time on recovering the clock of the transmitter and by using receiver's local clock).

As to claims 3 and 13, Ariyavisitakul further discloses that the distortion compensating further comprises: setting one or more parameter values based on the at least a portion of the at least one generated sampling (see Fig. 1, block 106, column 10, last paragraph and column 9, lines 33-35); and applying the one or more parameter values to the received input signal (see column 9, lines 35-38).

As to claims 9 and 19, Ariyavisitakul discloses that the communication channel is a digital communications channel (see the abstract and column 1, second paragraph).

As to claims 10 and 20, Ariyavisitakul discloses that the equalization is performed in accordance with a data receiver coupled to the communications channel (see column 10, last paragraph and the abstract).

As to claim 21, Ariyavisitakul discloses an equalization system responsive to an input signal received from a communication channel (see Fig. 1), comprising: a sampling module, the sampling module 104 (see column 10, last paragraph) generating at least one sampling from the received input signal (i.e. inherently by using a clock signal); and a filter (equalizer 107), the filter compensating for distortion associated with the communication channel based (see the abstract and column 10, last paragraph and column 1, lines 33-38) on an equalization algorithm which is responsive to at least a portion of the at least one sampling generated by the sampling module (see the abstract, lines 3-5). Ariyavisitakul discloses all the subject matters claimed in claim 21, except that the sampling clock is not related to the clock signal used to recover data associated with the received input signal. Yada, in the same field of endeavor, shows a system (see Figs. 1A and 1B) comprising a sampling device 4, an equalizer 5, a data detector 6, and a PLL circuit 7. Yada discloses that a sampling clock of frequency $F_s$, is supplied to ADC 4 to sample the input signal. Yada further discloses that the data detector 6 (interpreted as the recovery circuit) is supplied with a clock signal generated by a PLL circuit 7 (see column 8, last paragraph). Therefore Yada teaches that the sampling clock is not related to the clock signal used to recover data associated with the received input signal. It would have been obvious to one of ordinary skill in the art at the time of invention to use a clock for sampling the received signal unrelated to the clock used for data recovery purposes to make the process of data recovery faster (i.e. without spending time on recovering the clock of the transmitter and by using receiver's local clock).

As to claim 22, Ariyavisitakul further shows that the equalization system is part of a data receiver (see Fig. 1).

As to claim 23, Yada discloses that the equalization system 5 is independent of a clock and data recovery system 6 of the data receiver (see Figs. 1A and 1B).

Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ariyavisitakul and Yada, further in view of Hsu et al. (hereafter, referred as Hsu) (US 2004/0062329).

As to claims 2 and 12, Ariyavisitakul discloses that demodulator 104 oversamples the IF signal at a multiple of the symbol rate since optimum time for sampling the signal is unknown. Ariyavisitakul and Yada are silent in disclosing that the sampling (oversampling) generation step comprises the steps of: generating multiple phases of the sampling clock signal; and sampling the received input signal at the respective multiple phases of the sampling clock signal to generate respective multiple samples. Hsu, in the same field of endeavor, discloses an apparatus (see Fig. 1) comprising an oversampler 24 that samples the data using multiple clocks 26, producing 4 sampled signals. Hsu further discloses that the clocks are generated by a VCO 30 and are clocks of the same frequency and four different phases (see paragraph 0003). It would have been obvious to one of ordinary skill in the art at the time of invention to use multiple phases of a sampling clock to sample the input signal and determine the optimum clock for sampling the incoming data (see paragraph 0003) as suggested by Hsu.

Claims 4 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ariyavisitakul and Yada, further in view of Dally et al. (hereafter, referred as Dally) (US 2003/0086339).

As to claims 4 and 14, Ariyavisitakul and Yada are silent in disclosing that the sampling clock signal has a lower frequency than the data recovery clock signal. Dally, in the same field of endeavor, discloses a clock recovery circuit wherein the sample clock is slower (interpreted as having lower frequency) than the data clock (see paragraph 0060). It would have been obvious to one of ordinary skill in the art at the time of invention to make the sample clock slower than the data clock to maintain the synchronization between two clocks (data clock and sample clock) as suggested by Dally (see paragraph 0061) and recover the data.

Claims 5, 6, 8, 15, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ariyavisitakul and Yada, further in view of Shattil (US 2004/0243258).

As to claims 5 and 15, Ariyavisitakul and Yada disclose all the subject matters claimed in claims 1 and 11, except for validating the at least one generated sampling. Shattil discloses a receiver (see Fig. 10) comprising: a sampler 1002 to provide samples to selector 1004, wherein the selector provides weights to the samples (interpreted as validating the samples) (see paragraph 0124). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Ariyavisitakul and Yada as suggested by Shattil to select only samples which their power levels meet a predetermined threshold to enhance the integrity of the output signal.

As to claims 6 and 16, Shattil further discloses comparing samples of the at least

one generated sampling to a validation threshold (see paragraph 0124). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Ariyavisitakul and Yada as suggested by Shattil to select only samples which their power levels meet a predetermined threshold to enhance the integrity of the output signal.

As to claims 8 and 18, Shattil further discloses discarding samples of the at least one generated sampling that are determined to be invalid (see paragraph 0124). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Ariyavisitakul and Yada as suggested by Shattil to enhance the integrity of the output signal.

Claims 7 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ariyavisitakul, Yada, and Shattil, further in view of Best et al. (hereafter, referred as Best) (US 6,570,944).

As to claims 7 and 17, Ariyavisitakul, Yada, and Shattil disclose all the subject matters claimed in claims 5 and 15, except for generating leading edge samples and trailing edge samples from the received input signal; and varying an eye center threshold to determine the validity of the at least one generated sampling. Best, in the same field of endeavor, disclose an apparatus that reduces sampling errors for data communicated between devices (see the abstract). Best disclose that in any high-speed signaling system, the ability of the receiving device to sample the data signal at a precise instant within the valid data interval (the “data eye”) is often a critical factor in determining how brief the data eye may be. Best further discloses that any technique for

more accurately controlling the sampling instant within the data eye generally permits faster data transfer and therefore higher signaling bandwidth. Best further shows generating leading edge samples and trailing edge samples from the received input signal (see Fig. 2) and delaying the signal so that the delayed signal transitions at the midpoint of the data eye (interpreted as varying an eye center threshold to determine the validity of the at least one generated sampling). Therefore, for the reasons stated above, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ariyavisitakul, Yada, and Shattil as suggested by Best.

**(10) Response to Argument**

(A) Introduction

Prior to responding to the arguments, the examiner would like to describe the field of invention.

The invention relates to a method/apparatus for equalizing an input signal received from a communications channel. At least one sampling is generated from the received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal. Distortion associated with the communications channel is then compensated for based on at least a portion of the at least one generated sampling.

(B) Response to Arguments(s)

The examiner discusses the claims in the same order as the appellant.

Claims 1, 3, 9-11, 13, and 19-22-

Appellants argue (see page 6, lines 11-26) that Ariyavisitakul fails to anticipate the limitation of the clock signal that is the basis of generating at least one sampling being unrelated to a clock signal used to recover data, since in Ariyavisitakul, the symbol timing and the optimum sampling time are the same.

In response to Appellants argument, Examiner asserts that as cited in the previous Office Action, Ariyavisitakul discloses all the subject matters claimed in claim 1, except that the sampling clock is not related to the clock signal used to recover data associated with the received input signal. However, reference Yada has been used to reject the above-noted limitation. Therefore, reference Ariyavisitakul has not been used by the Examiner to reject the above-noted limitation.

Appellants argue (see page 6, line 26—page 7, line 24) that Yada reference fails to teach or suggest “generating at least one sampling from the

received input signal based on a clock signal unrelated to a clock signal used to recover data associated with the received input signal". Appellants further argue that since the clock used by the data detector 6, in Yada reference, is extracted from the equalizer output signal which was sampled at the rate of clock Fs (ADC clock), therefore the two clocks are related.

In response to Appellants argument, Examiner asserts that as disclosed by Yada a sampling clock of frequency $F_s$, is supplied to ADC 4 to sample the input signal. Yada further discloses that the data detector 6 (interpreted as the recovery circuit) is supplied with a clock signal generated by a PLL circuit 7 (see column 8, last paragraph). Although, in column 8, lines 65-68, Yada discloses that PLL extracts a clock signal from the waveform equalized digitized audio signal, Yada does not indicate that the extracted clock is the clock used by ADC 4. Yada specifically states extracting a (and not the) clock signal from the waveform equalized digitized audio signal. Therefore the clock used by ADC 4 is not the clock used by data detector 6. Examiner further asserts that term "unrelated" as cited in claim 1, is a broad term and has not been specifically defined by the Appellants in the claim. Examiner would like to call the attention of the Appellants to the invention's disclosure where Appellants state that the "sampling clock signal may have a lower frequency than the data recovery clock signal" (see page 2, lines 16-17). This statement is the first statement presented by the Applicants to show that the clocks are unrelated. Yada does not teach away from this statement, because it shows that the clock signals are not

identical and therefore they may have different frequencies. The second statement provided by the Appellants regarding the clocks is on page 6, line 10, where Appellants state that the clocks are unrelated (e.g. independent). In this statement Appellants provide only an example for term "unrelated" and do not indicate that the clocks are necessarily independent. In rejection of claim 1, Examiner has given the claim (and term "unrelated") its broadest reasonable interpretation and believes that Yada reference reads on the limitation argued by the Appellants.

Appellants further argue (see page 8, line 8 – page 9, line 2) that Yada is not analogous prior art and therefore cannot form the basis for a rejection under 35 U.S.C §103.

Examiner respectfully disagrees. In response to Appellants' argument that Yada is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Yada is in the field of Appellants, endeavor (Yada discloses a data recovery device (see at least the abstract)), and it is pertinent to the particular problem with which the Appellant was concerned (i.e. using two different clocks for sampling and data recovery).

Appellants argue (see page 9, lines 3-16) that there has been no showing in the present rejection of claim 1 of objective evidence of record that would motivate one skilled in the art to combine the completely disparate teachings of Ariyavisitakul and Yada to produce the particular limitations in question.

Examiner asserts that, as cited in the last Office Action, it would have been obvious to one of ordinary skill in the art at the time of invention to use a clock for sampling the received signal unrelated to the clock used for data recovery purposes to make the process of data recovery faster. If the clocks are the same, data recovery circuit needs to extract the clock from the incoming signal before processing the signal. This process is time consuming. However, if the data recovery circuit has its own local clock, there is no need for extracting the clock and the incoming signal can be processed immediately by using the local clock. Reducing the time required for signal processing (here the data recovery process) is always desirable in communication systems and the teachings of Yada helps to reduce the processing time of the signal in the apparatus disclosed by Ariyavisitakul.

Appellants argue (see page 9, lines 26) that "the Office Action claims that using a clock signal is inherent in Ariyavisitakul. However, Ariyavisitakul does not contain the disclosure which is necessary to support a rejection of a claim on the basis of inherency.

Examiner respectfully disagrees. As discussed in the last Office Action, Ariyavisitakul discloses generating at least one sampling from the received input

signal (see block 104 and column 10, last paragraph). Since every sampling device known in the art needs to have a clock in order to function properly (sample the signal) and it is impossible to sample a signal without using a sampling clock, therefore it is a valid statement to say that sampling device 104 inherently has a sampling clock.

Claim 23-

Appellants further argue (see page 10, lines 22) that Yada fails to disclose limitation “the equalization system is independent of a clock and data recovery system of the data receiver", because in Fig. 1 Yada clearly shows an arrangement in which equalizer 5 is coupled to data detector 6.

Examiner asserts that, as evidence by Appellants’ invention disclosure, term “independent” does not indicate that the units have not been coupled together. Examiner would like to call the attention of the Appellants to Fig. 4 of invention's disclosure, where Appellants show that the output of equalizer 400 has been passed to the data recovery circuit. Examiner has interpreted term "independent" as units being distinct from each other and Yada clearly shows (see Figs. 1A and 1B) that equalizer 5 and data detector 6 are distinct units.

Claims 4 and 14-

Appellants argue that relied upon portion of Dally in fact teaches away from the limitation "the sampling clock signal has a lower frequency than the data

recovery clock signal" by suggesting that an undesirable "phase lag" occurs when the sample clock is slower than the data clock.

Examiner asserts that Dally in paragraph 0061 discloses that when the input data frequency is slightly faster (slower) than the reference clock frequency and the input signal has significant jitter, the sample point will lag (lead) the correct value so that the early/late probabilities are unbalanced by an amount large enough to generate sufficient net early (late) edges to adjust the clock position often enough to keep up with the constant phase drift between the two clocks. Therefore, as cited in the previous Office Action, it would have been obvious to one of ordinary skill in the art at the time of invention to make the sample clock slower than the data clock to maintain the synchronization between two clocks (data clock and sample clock) as suggested by Dally (see paragraph 0061) and recover the data.

Claims 2, 5-8, 12, and 15-18- Appellants do not argue the individual limitations of dependent claims 2, 5-8, 12, and 15-18. Therefore the response to arguments for claims 2, 5-8, 12, and 15-18 is the same as the response to the argument of claim 1 stated above.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/L. M./

/Leila Malek/

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